Multi-Objective Univariate Marginal Distribution Optimisation of Mixed Analogue-Digital Signal Circuits

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ABSTRACT
Design for specific customer service plays a crucial role for the majority of the market in modern electronics. However, adaptability to an individual customer results in increasing design costs. A key to manage these opposite requirements is a wide application of computer aided design tools for multi-objective optimisation of existing IP blocks. In this paper we introduce a new approach to multi-objective optimisation of mixed analogue-digital signal circuits on the base of the univariate marginal distribution algorithm. Practical illustration of the use of this approach is demonstrated for an industrial electronics application design. Experiments indicate that multi-objective optimisation of mixed analogue-digital signal circuits on the base of the univariate marginal distribution algorithm meets different design specifications.

Categories and Subject Descriptors
J. 6 [**Computer-Aided Engineering**]: Computer-Aided Design

General Terms
Algorithms, Performance, Design

Keywords
Evolutionary probabilistic models, circuit optimisation, multi-objective optimisation

1. INTRODUCTION
Time-to-market, cost, and specific customer cervices became prevailing factors in the increasing global realm of modern electronics. Simultaneous requirements of miniaturization result in an increasing level of design complexity to meet all opposite design requirements. A key to the satisfaction of design requirements is a wide application of computer aided design tools.

Commercial circuit optimisation tools (NeoCircuit, Circuit Explorer, MunEDA, etc.) support optimisation at cell level. However, a design based on fully optimised library cells may fail to meet all design specifications at the system level. It results in additional iterations during design cycle and increasing design cost.

Mixed analogue-digital signal circuits play an important role in different applications in telecommunication, automotive electronics, etc. In this paper, we focus on the application of the univariate marginal distribution algorithm (UMDA) to multi-objective optimisation of mixed analogue-digital signal circuits at the system level.

The UMDA has been applied to design of analogue circuits, e.g. [14]. Note, that evolutionary probabilistic models work on mesoscopic level [15]. They select individuals on microscopic level, whilst they generate new solutions using marginal distribution. Note that the marginal distribution is macroscopic variable. It allows to accumulate the information about perspective regions of the fitness function landscape and to find reasonable solutions quickly [15]. In this paper the approach [14] is expanded to multi-objective optimisation of mixed analogue-digital circuits at the system level. We use the symmetry recognition circuit as our benchmark. This circuit is used in an industrial electronics system based on piezoelectric transformer application [3, 20]. We compare the effectiveness of the classical UMDA and its modification by elitism for static fitness schedule.

The outline of the paper is as follows. Section 2 briefly summaries some recent results in circuit design and optimisation research. Section 3 presents our approach. We discuss our results in Section 4. Conclusions are presented in Section 5.

2. RELATED WORKS
The computer-aided design of integrated circuits is not trivial. Cheap and reliable chips should have small area and meet all design specifications.

Usually a design flow of mixed analogue-digital signal circuits is based on design experience. It results in long design cycle and high human efforts. Even insignificant changes in design requirements may result in long iterations to adapt the initial design to new customer requirements. The main bottleneck is analogue circuits design [8].

Knowledge–based analogue design approaches are complex for formalization. Therefore, they failed in computer-aided design applications [8].

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An alternative approach to analogue circuit computer-aided design is based on different optimisation techniques. It includes OPTIMAN [9], MAELSTROM [12], ASF [13], ASTRX/OBLX [21], ANACONDA [22], etc. They differ by the circuit performance evaluations and by the search algorithm. OPTIMAN [9] uses analytical models that are fast, but their accuracy is better for small-signal characteristics. Another approach is based on numerical simulation in the loop of the optimisation. MAELSTROM [12] and ANACONDA [22] use SPICE, while ASTRX/OBLX [21] exploits the asymptotic evaluation. ASF [13] combines SPICE and the analytical approaches. Simulated annealing and its different modifications are mainly used in the tools mentioned above [9, 13, 21]. A combination of genetic algorithms and simulated annealing in MAELSTROM [12] allows to enhance design capabilities. The genetic optimisation of circuits based on matching properties of devices [2] provides circuit tolerance to process variations. A novel algorithm based on combination of evolutionary strategies and simulated annealing optimises analogue circuit characteristics [2].

The approach [12] has been used in the commercial tool NeoCircuit at Neolinear Inc., now acquired by Cadence. Another commercial tool leveraging intelligent systems techniques supports multiobjective optimisation formulation (AMS Genius at Analog Design Automation, now acquired by Synopsys). The commercial tool WiCkeD [1] is based on numerical optimisation algorithms. However, these tools are available for optimisation at the cell level only.

In [16] hierarchical approach to analogue circuit design based on VHDL-AMS has been proposed. However, mutual influence of fully optimized library circuits has not been considered. Approximation of circuit performances is the backbone for analogue platform–based design of mixed signal circuits [4]. However, long simulation time is required for characterization of each component supported by the platform.

The DAISY tool optimises discrete–time [6] and continious-time [10] $\Delta\Sigma$ modulators, based on the differential evolution algorithm and the fast dedicated $\Delta\Sigma$ behavioural simulator. However, the run times remain long [7].

Therefore, design efficiency is the main obstacle in effective circuit design. Up to date, there is no a method to resolve the problem if the system does not meet design specifications [11]. In the worst case, the complete redesign may be required. It increases the time to market and the development cost.

Evolutionary computation is widely used for computer-aided design as design automation tools at various levels of abstraction. In this paper we restrict our discussion to multi-objective optimisation of mixed analogue-digital signal circuits at the system level.

A design of a system with hundreds of transistors is too complex to attack at once. A long simulation run-time is another crucial obstacle. Smart algorithms are required to manage the complexity of the problem. They should be able to find a good solution with reasonable computational costs.

Evolutionary probabilistic models have been recognized as a new computing paradigm in evolutionary computation. Evolutionary probabilistic models include the estimation of distribution algorithms, probabilistic model building genetic algorithms, ant colony optimisation, cross entropy methods. There is no traditional genetic algorithms crossover or mutation in evolutionary probabilistic algorithms. Instead, they explicitly extract global statistical information from their previous search and build a probability distribution model of promising solutions, based on the extracted information. New solutions are sampled from the probabilistic model. Probabilistic evolutionary algorithms represent a new systematic way to solve hard search and optimisation problems. They have shown to resolve a number of problems the conventional genetic algorithms experience great difficulties with and solve a number of difficult problems quickly, accurately, and reliably [15].

The Estimation of Distribution Algorithms EDA has been proposed by Mühlenbein and Paaß [18] as an extension of genetic algorithms. Instead of performing recombination of strings, EDA generate new points according to the probability distribution defined by the selected points. In [17] Mühlenbein showed that genetic algorithms can be approximated by an algorithm using univariate marginal distributions only. UMDA is an evolutionary probabilistic models algorithm, which combines mutation and recombination by means of distribution. The distribution is estimated from a set of selected points. It is used then to generate new points for the next generation. In order to improve design abilities, mutation has been introduced into UMDA by a concept called Bayesian prior [15]. UMDA with Bayesian prior is able to overcome local minima [15]. Furthermore, the experimental research in order to make a reasonable choice of Bayesian prior for analogue circuit design [19] and an effective circuit representation [23] was used. Moreover, analogue circuits that are better than those produced by an expert circuit designer have been synthesized [14].

In this paper the approach [14] is expanded to multi-objective optimisation of mixed analogue-digital signal circuits at the system level. Note that we restrict our research to the static technique of fitness function evaluation only.

3. OVERVIEW of MULTI-OBJECTIVE OPTIMISATION of MIXED ANALOGUE-DIGITAL CIRCUITS BASED on the UMDA

The design strategy used in our design flow is a performance- and area-driven concurrent top-down down-up methodology. To tract complexity, a large design is broken up into a set of subblocks, until all blocks are at transistor level. These low-level blocks are sized to be optimal. Then performance of the complete systems is checked. If it does not meet all specifications then optimisation at the system level and at the transistor level is done simultaneously. In the final optimisation loop the design space includes only crucial circuit parameters (for example, the transistors' widths and lengths, values of independent voltages sources, etc.). They are given by a user.

The design flow supported by our approach consists of design steps sequence (Fig. 1). Below we describe the design flow in more details.

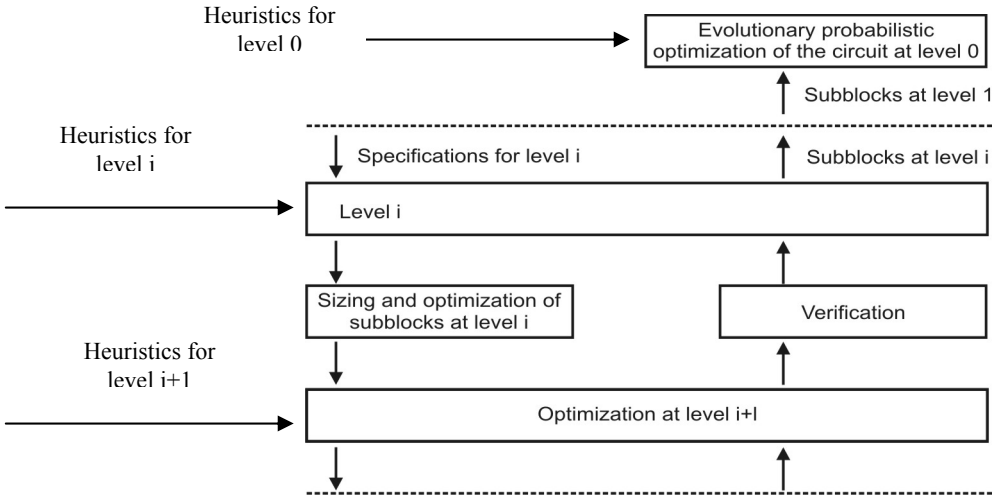


Figure 1. A concurrent design flow supported by our approach

First, a large design is cut into a set of subblocks. If they include no primitive components, they are designed and optimised firstly. Second, all subblocks are synthesized. Third, a user defines a set of crucial circuit parameters and device relationships (matching, ratio between transistors widths, etc.). Their acceptable variations range is given by a user as well. Finally, optimisation at system level is done. Pareto optimal fitness function is used for high quality design.

Optimisation at low hierarchical levels can be performed either by a commercial tool or by the UMDA. The final optimisation is performed by the UMDA.

We use the linear circuit representation according to recommendations [23]. A genotype is formed by means of the combination of separate genes for each variable component (a transistor, an independent voltage source, etc.). Briefly, each gene consists of alleles for value parameters. Fig. 2 shows the general structure of our circuit representation.

The UMDA [15] combines mutation and recombination by using probabilistic distribution. A set of selected points M is used to estimate the distribution. Our focus is on the truncation selection, where $\tau = M/N$ is the amount of selected individuals, N is the population size. Note that we use truncation selection because of its simplicity. Selected individuals are then used to generate N new points for the next generation according to the probability $p(X, t)$ in the population at the generation t

$$p(X,t) = \prod_{i=1}^{n} p_i^s(x_i,t)$$

where $p_i^s(x_i,t)$ are marginal frequencies;

n is equal to the genotype length.

n is calculated as follows:

$$n = \sum_{i=1}^{N_p} (Max_i - Min_i)/D_i ,$$

where Max_i and Min_i are equal to the maximal and minimal acceptable value of parameter i, respectively;

D_i is equal to the incremental value of parameter i;

N_p is a number of varying parameters.

UMDA [15]

Step 1. Set t=1. Generate N possible design solutions randomly.

Step 2. Select $M < N$ solutions according to a selection method.

Step 3. Compute marginal frequencies $p_i^s(x_i,t)$ of the selected set.

Step 4. Generate N new solutions according to the marginal distribution $p(X,t+1) = \prod_{i-1}^{n} p_i^s(x_i,t)$. Set $t=t+1$.

Step 5. If termination criteria are not met, go to Step 2.

We use mutation settings according to recommendations [19].

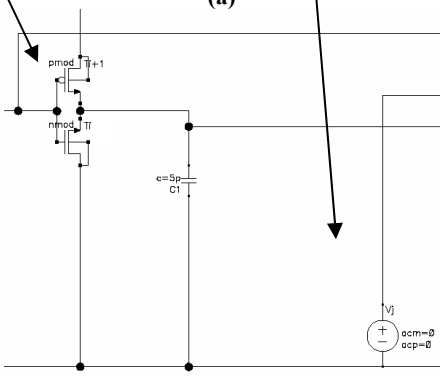
The decision as to how many iterations should be done and evaluated can be based upon several factors such as termination conditions of an optimisation algorithm used, certain metric factor, a time/effort factor of wanting to generate a circuit with better metrics. A subjective factor where an experienced circuit designer decides when to stop additional iterations based on the designer's experience in circuit design can be used as well.

4. EXPERIMENTAL RESULTS

The proposed approach to evolutionary probabilistic optimisation of mixed analogue-digital signal circuits based on the UMDA has been prototyped in a software framework EvolCircuit. We have integrated in one system an existing in-house tool for simulation TITAN [5] and a new tool for probabilistic evolutionary circuit optimisation based on the UMDA. The system supports a combination of standard cells and custom cells. Standard cells

…	Transistor i		…	Independent voltage source j	…
…	Width	Length	…	Value	…
…	101..	01..	…	1110…	…

(a)



(b)

Figure 2. a) Chromosome and b) the parameters of the circuit elements, created from it

represent cells that have been designed previously by the third party and have been included in a cell library. Note that we use library cells that have been optimised by WiCkeD tool [1] and proved in silicon. Therefore, we do not change their parameters. Our focus is only on variations of crucial circuit parameters (transistors widths and lengths, values of independent voltage sources, etc.).

Our circuit design benchmark chosen is a symmetry recognition circuit included in a driving circuit concept of a piezoelectrical transformer power converter [3, 20]. It contains more 800 transistors, including analogue-digital converters, comparators, flip-flops, etc. Fig. 3 illustrates some key features of symmetry recognition.

Although we illustrate our approach for the symmetry recognition circuit it can be easily expanded to different applications areas of electronic systems (automotive electronics, telecommunication, etc.). Note, that the correspondent service for new features should be added to the software framework by application engineers.

The symmetry recognition circuit has been designed by a human designer for another design performance. We have applied our approach to reach new design goals and to minimize chip area. The input specification for the symmetry recognition design benchmark is summarized in Table 1.

Optimisation problem is given as follows:

$$\min f(X) = (f_1(X), f_2(X)), \quad X \in \Omega,$$

where $X = (x_1, \ldots, x_m)$ is a real variable vector, Ω is the feasible solution space. For the evaluation of the fitness function $f_1(X)$ the values of the standard deviations of symmetry recognition are calculated across evaluation points Nc

$$f_1(X) = \max\{\sqrt{\frac{1}{N_C}\sum_{i=1}^{N_C}(f_i - \bar{f}_{0.8})^2}\,|_{\frac{T_1}{T_2}=0.8};$$

$$\sqrt{\frac{1}{N_C}\sum_{i=1}^{N_C}(f_i - \bar{f}_{0.9})^2}\,|_{\frac{T_1}{T_2}=0.9}\}$$

$$\bar{f}_k = \frac{1}{N_C}\sum f_i\,|_{\frac{T_1}{T_2}=k}, k = 0.8; 0.9$$

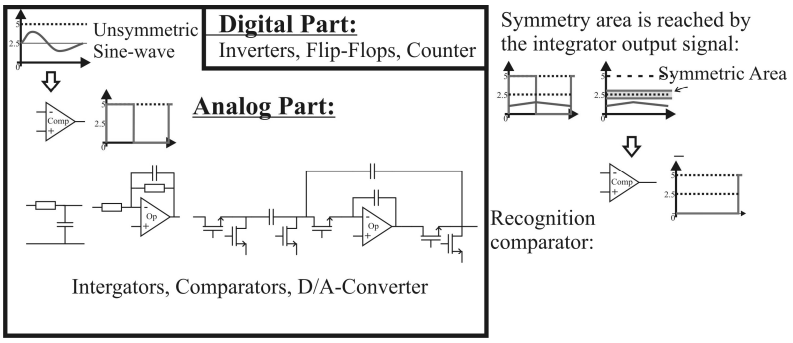


Figure 3. Load-symmetry recognition circuit principle of a sine-wave

Table 1. Input specifications for our symmetry recognition design benchmark

Circuit Specifications	Values
Frequency range	25 kHz – 500 kHz
Evaluation points	25 kHz, 125 kHz, 250 kHz, 500 kHz
Time asymmetry coefficient T_1/T_2	0.8; 0.9; Δ 0.01
Variations of DC voltage source	0.8 -2 V; Δ 0.1 V
Transistor length	1.5 -9.9 μm; Δ 0.3 μm
Transistor width of P-channel current mirror	5.3 -18.1 μm; Δ 0.1 μm
Par_2	1.0 -2.0; Δ 0.02

where f_i is the recognition asymmetry;

the fitness function $f_2(X)$ is evaluated as follows:

$$f_2(X) = \sum_{k=1}^{N_p} f_{pk}(X) + \sum_{k=1}^{N_n} f_{nk}(X),$$

where f_{pk} and f_{nk} are P- and N-transistors area according to the technology B6CA, respectively;

N_p and N_n are equal to the number of P- and N-transistors in a given netlist, respectively.

We assume that asymmetry has been recognized after the output voltage of the symmetry recognition circuit [3, 20] is below 1 V. 100% performance value of symmetry recognition circuit is achieved when asymmetry has been recognized at all evaluation points.

The stopping criterion is a finding a circuit with chip area that is equal to minimal chip area according to technology constraints or computational costs exceed a given limit.

Out technology is the Infineon BiCMOS technology B6CA. We use the correspondent B6CA transistors models. However, EvolCircuit can be expanded for different technologies easily by application engineers.

Design heuristic are given as follows:

- The lengths of all transistors are equal to *l*.

- The widths of the transistors of current mirrors are equal.

- The width of the transistor of the current source should be set to w/V_g, where *w* is the width of the transistors of P-channel current mirror. In our experiments we set V_g to 2.1 as a relationship between the currents of the symmetry recognition circuit.

- The width of the transistors of inverters should be set to $w/2$.

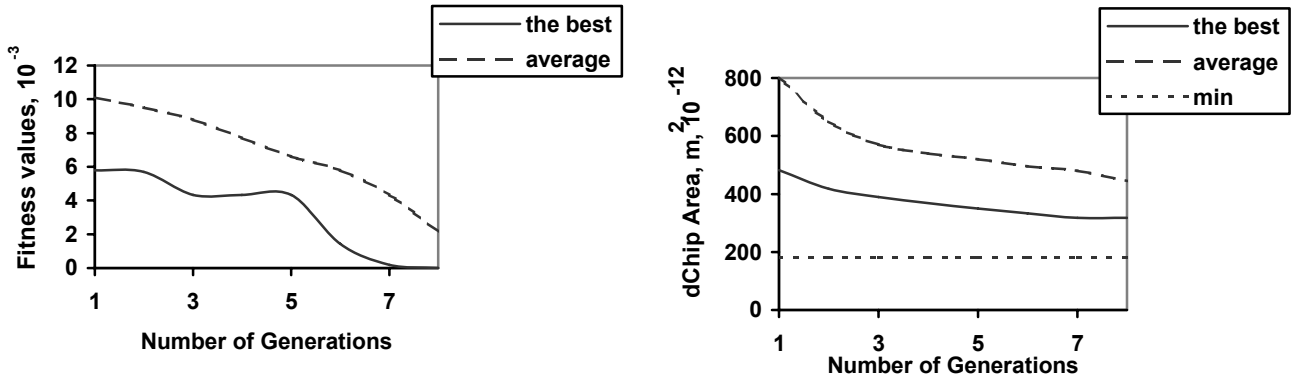
- The width of the transistors of N-channel current mirror should be set to

$$w_N = \begin{cases} Par_2 * w, & w_N < 20 \quad \mu m \\ 20 \quad \mu m, & w_N \geq 20 \quad \mu m \end{cases}$$

where w_N is the transistor width of N-channel current mirror.

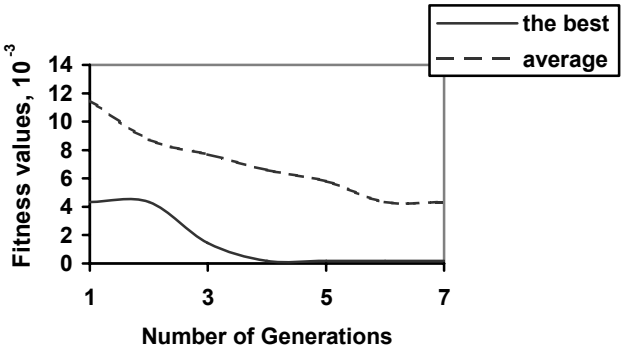
Note, that we restrict our design space according to the technology B6CA constraints in order to avoid incorrect solutions.

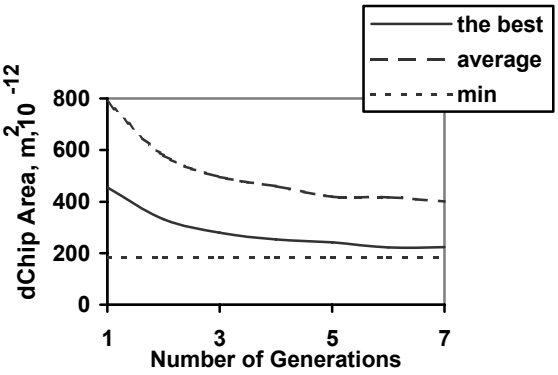
We examined the behaviour of different algorithms for the fixed number of bits *n*=22 with a truncation threshold τ from 0.2 to 0.5. Population size changes from *N*=4 to *N*=10. Figures 4 -7



(a) **(b)**

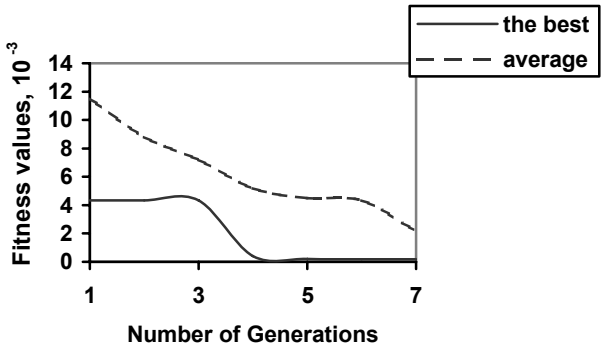
Figure 4. Performance (average of 10 runs) behaviour of classical UMDA for population size N=4 and truncation selection with τ=0.5 a) for deviations of symmetry recognition b) for chip area variations in microns.

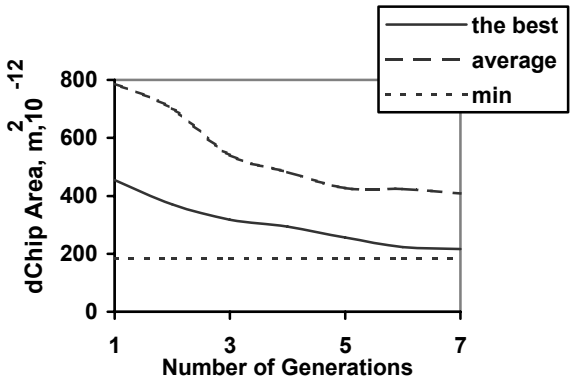




(a) (b)

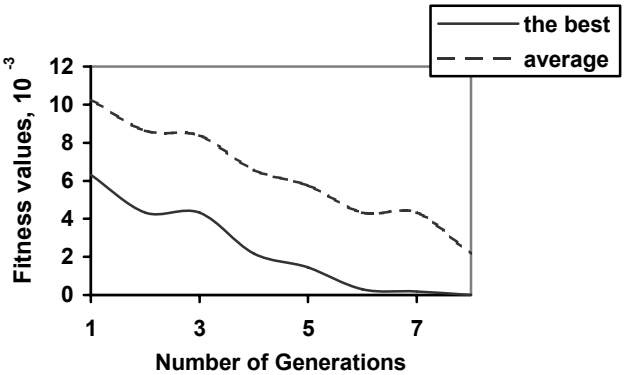
Figure 5. Performance (average of 10 runs) behaviour of classical UMDA for population size N=10 and truncation selection with τ=0.2 a) for deviations of symmetry recognition b) for chip area variations in microns.

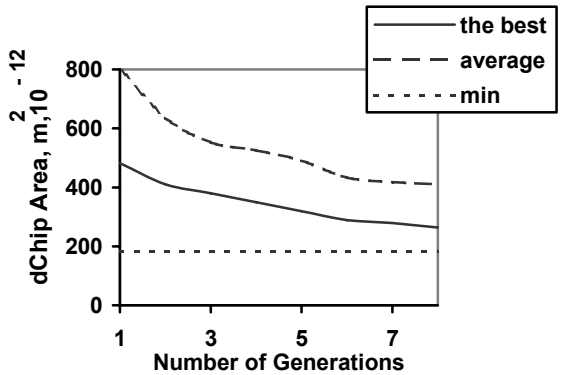




(a) (b)

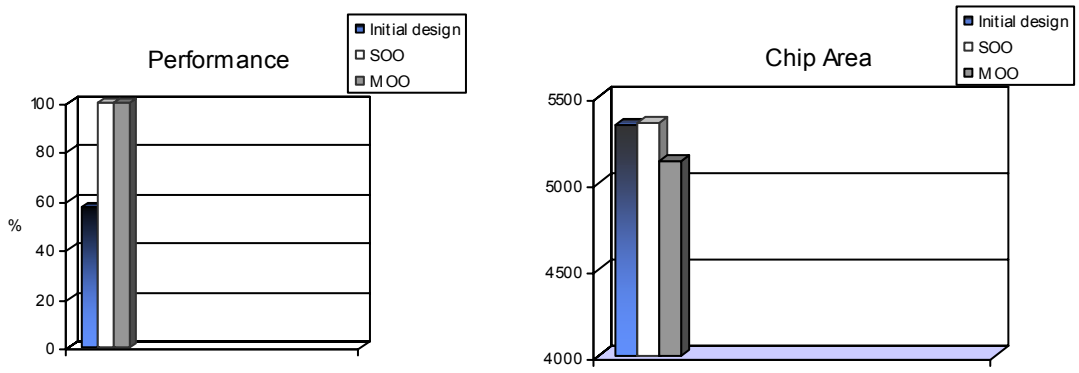
Figure 6. Performance (average of 10 runs) behaviour of classical UMDA for population size N=10 and truncation selection with τ=0.5 a) for deviations of symmetry recognition b) for chip area variations in microns.





(a) (b)

Figure 7. Performance (average of 10 runs) behaviour of UMDA with elitism for population size N=4 and truncation selection with τ=0.5 a) for deviations of symmetry recognition b) for chip area variations in microns.



(a) **(b)**

Figure 8. A comparison for different circuits a) performance and b) chip area in microns

show how the best and average fitness functions and the best and average chip area are changed when algorithms settings are modified. The line **min** shows minimal chip area according to the technological restrictions. Figures 4, 6 illustrate the case in which the population size varies between N=4 and N=10 and the truncation threshold is equal to τ=0.5. Figure 5 shows the case in which the population size is fixed N=10, whilst the truncation threshold is decreased to τ=0.2. Note that we use these population sizes to find a compromise between computational costs and obtaining reasonable results.

The most obvious fact is that the optimisation speed is generally enhanced where larger population sizes and smaller truncation selection threshold are used. Therefore, for multi-objective circuit optimisation we should use larger population size in despite of higher computational costs.

In order to enhance design capabilities we have introduced elitism in evolutionary process. Figure 7 illustrates the case in which the population size is equal to N=4 and the truncation threshold is equal to τ=0.5. It is obvious that that elitism allows to increase an efficiency of evolutionary search.

During evolutionary runs the required design specifications have been met. The best circuit has the required standard deviations of symmetry recognition and smaller chip area. Fig. 8 shows the performance of symmetry recognition and the chip area of the initial and the optimised circuits. Bar 1 shows the best initial circuit characteristics, bar 2 shows the best results of single-objective optimisation (SOO) [24], bar 3 shows the best results of multi-objective optimisation (MOO).

It is obvious that multi-objective optimisation of mixed analogue-digital signal circuits based on the UMDA is able to find a circuit with the required design specifications and smaller chip area.

5. CONCLUSIONS

In this paper the application of the UMDA to multi-objective optimisation of mixed analogue-digital signal circuits was presented. The objective was to apply smart algorithms, e.g. evolutionary probabilistic models, in industrial design practice, e.g. to optimise existing IP blocks. It was shown that both classical UMDA and its modifications with elitism can be used to meet new design performance and to minimize chip area. It seems that the UMDA with higher population sizes is more suitable for multi-objective optimisation of mixed analogue-digital signal circuits. Advantages of this approach are the overcoming design problems and meeting design goals.

The approach was validated by optimising the symmetry recognition circuit containing analogue-digital converter, flip-flops, comparators, etc. Experimental results validate the methodology by comparing the performance of the optimised circuits with the initial circuit.

In this paper the results of circuit performance optimisation and minimisation of chip area have been discussed. However, industrial design practice expects high yield of an optimised solution as well. In the future research we will expand our approach to optimise a given design for manufacturability as well.

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7. REFERENCES

[1] Antreich, K., Pronath, M., et al. WiCkeD: Analog Circuit Synthesis Incorporating Mismatch. In *CICC 2000*. 2000.

[2] Aplaydin, G., Balkir, S., Dündar, G. An Evolutionary Approach to Automatic Synthesis of High-Performance Analog Integrated Circuits. *IEEE Transactions on Evolutionary Computation 3* (2003), 240–252.

[3] Bisogno, F.E., Nittayarumphong, S., Radecker, M. et al. Dynamic Modeling of Class-E Resonant Converter for Step-Down Applications Using Piezoelectric Transformers. In *Proc. IEEE PESC2005*. 2005, 2797-2803.

[4] De Bernardinis, F., Nuzzo, P., Sangiovanni Vincentelli, A. Mixed Signal Design Space Exploration through Analog Platforms. In *Proceedings of DAC 2005*. 2005, 875-880.

[5] Feldmann, U., Wever, U., Zheng, Q., Schultz, R., Wriedt, H. *Algorithms for modern circuit simulation*. Archiv für Elektronik und Übertragungstechnik 46, 1992.

[6] Francken, K., and Gielen, G. A high-level simulation and synthesis environment for delta-sigma modulators*. IEEE Trans. Comput.-Aided Des., 22*, 8 (2003), 1049–1061.

[7] Gielen, G. G. E. CAD tools for embedded analogue circuits in mixed-signal integrated systems on chip, *IEE Proc.-Comput. Digit. Tech., 152*, 3 (May 2005), 317- 332.

[8] Gielen, G. G. E., Rutenbar, R. A. Computer-Aided Design of Analog and Mixed Signal Integrated Circuits. *Proc. of the IEEE 12* (2000), 1825-1852.

[9] Gielen, G. G. E., Walscharts, H. C. C., and Sansen W. M. C. Analog circuit design optimization based on symbolic simulation and simulated annealing. *IEEE J. Solid-State Circuits, 25, 3* (Jun. 1990), 707–713.

[10] Gielen, G., Francken, K., Martens, E., and Vogels, M. An analytical integration method for the simulation of continuous-time DS modulators, *IEEE Trans. Comput.-Aided Des., 23*, 3 (2004), 389–399.

[11] Gielen, G., McConaghy, T., Eekelaert, T. Performance Space Modeling for Hierarchical Synthesis of Analog Integrated Circuits. In *Proceedings of DAC 2005*. 2005, 881-886.

[12] Krasnicki, M., Phelps, R., Rutenbar, R. A., Carley, L. R. Maelstrom: Efficient Simulation-Based Synthesis for Custom Analog Cells. In *Proceeding ACM/IEEE DAC*. 1999.

[13] Krasnicki, M.J., Phelps, R., Hellums, J.R., McClung, M. Rutenbar, R.A. Carley, L.R. ASF: a practical simulation-based methodology for the synthesis of custom analog circuits, In *Proceedings of ICCAD 2001*. 2001, 350–357.

[14] Muehlenbein, H., Kureichik, V.M., Mahnig, T., Zinchenko L.A. Application of the Univariate Marginal Distribution Algorithm to Analog Circuit Design. In *Proceedings of the Evolvable Hardware Conference (EH '02).* 2002, 93-101.

[15] Muehlenbein, H., Mahnig, T. Evolutionary Computation and Wright's equation. *Theoretical Computer Science, 287* (2002), 145-165.

[16] Mueller, D., Stehr, G., Graeb, H., Schlichtmann, U. Deterministic Approaches to Analog Performance Space Exploration. In *Proc. DAC 2005*.2005, 869–874.

[17] Mühlenbein, H. The Equation for Response to Selection and its Use for Prediction. *Evolutionary Computation, 5* (1998), 303-346.

[18] Mühlenbein, H., Paaß, G. From Recombination of Genes to the Estimation of Distributions. In *PPSN IV*. LNCS, Vol. 1141, Springer-Verlag, 1996, 178-187.

[19] Mühlenbein, H., Zinchenko, L.A., et al. Effective Mutation Rate of Probabilistic Models for Evolutionary Analog Circuit Design. In *Proc. IEEE ICAIS 2002*. 2002, 401-406.

[20] Nittayarumphong, S., Bisogno, F.E., Radecker, M., et al. Dynamic behaviour of PI controlled Class-E Resonant Converter for Step-Down Applications Using Piezoelectric Transformers. In *Proc. EPE2005*. 2005.

[21] Ochotta,, E. S., Rutenbar, R. A., and Carley, L. R. Synthesis of high-performance analog circuits in ASTRX/OBLX. *IEEE Trans. Computer-Aided Design Integr. Circuits Syst., 15, 3* (1996), 273–294.

[22] Phelps, R., Krasnicki, M., Rutenbar, R. A., Carley, L. R., and Hellums, J. R. ANACONDA: Simulation based synthesis of analog circuits via stochastic pattern search. *IEEE Trans. Computer-Aided Design Integr. Circuits Syst., 19, 6* (Jun. 2000), 703–717.

[23] Zinchenko, L.A., et al. A Comparison of Different Circuit Representations for Evolutionary Analog Circuit Design. In Proc. *ICES (ICES '03)*. Springer-Verlag, 2003, 13-23.

[24] Zinchenko, L.A., Radecker, M., Bisogno, F. Application of the Univariate Marginal Distribution Algorithm to Mixed Analogue - Digital Circuit Design and Optimisation. In *Proceedings of EvoWorkshops*. Lecture Notes in Computer Science, 2007, 431-438.