Specialized Hardware for Implementation of Evolutionary Algorithms

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1 Hardware Description

Evolutionary Algorithms (EAs) are getting more and more popular and many successful applications of these principles have been reported. One of the major drawbacks of these approaches in general is that they are often not competitive with respect to runtime in comparison to other methods. A natural way to speed up these algorithms and to handle large problem instances are parallel implementations of EAs on parallel hardware.
We present a dynamically reconfigurable *Multiprocessor System* (MPS). Small RISC type CPUs, the so called *Processor Nodes* (PNs), are the basic computing units of the system. The communication channels between the PNs can dynamically be switched by a *Field Programmable Interconnection Device* (FPID), realizing a crosspoint switch. The FPID is controlled by a seperated *Communication Processor* (CP). Up to 9 PNs fit onto one carrier board, which is a long PC ISA card. A picture of the layout is given in Figure 1, for more details see (P. Biermann, 1997).
For the use in the field of EAs also the software framework plays a major role. We developed a software environment that is based on C and assembler language. The use of machine code ist integrated to speed up time critical applications, see also (T. Schubert et al., 2000).

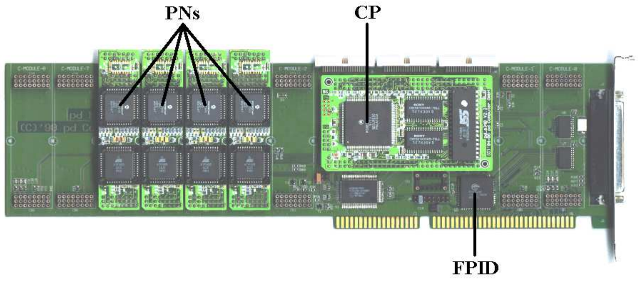

Figure 1: Layout of the carrier board

2 A Case Study

As a first application we consider the symmetric *Travelling Salesman Problem*. For the experiments we used a configuration of the carrier board with 4 PNs and an EA as the underlying optimization procedure. After each 100st generation the best elements are exchanged between the PNs. The results obtained are given in Table 1 in the last column. The second column describes the results obtained by a reimplementation of the same algorithm on a *Sun Ultra Sparc 1*.
As can be seen, in almost all instances the results of the *Multiprocessor System* outperform the reimplementation, showing the high performance of our approach.

Table 1: Symmetric travelling salesman problems

	Unix version	**MPS**
#cities	shortest tour	shortest tour
28	594.8	594.8
40	546.8	537.5
60	782.5	782.5
100	1431.2	1422.3
140	1605.9	1605.9

References

P. Biermann, R. Drechsler, B. Becker. 1997. Modularity as key element in modern system design - a case study for industrial application of parallel processing. *European Design & Test Conf. User Forum*, pp 15–20.

T. Schubert et al. 2000. Specialized hardware for implementation of evolutionary algorithms. *Technical Report*. Albert–Ludwigs–University of Freiburg.